A low-offset low-voltage CMOS Op Amp with rail-to-rail input and output ranges

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Abstract - **A low voltage CMOS op amp is presented. The circuit uses complementary input pairs to achieve a rail-to-rail common mode input voltage range. Special attention has been given to the reduction of the op amp's systematic offset voltage. Gain boost amplifiers are connected in a special way to provide not only an increase of the low-frequency open-loop gain but also a significant reduction of the systematic offset voltage.**

I. Introduction

The input offset voltage of a practical operational amplifier consists of a random and a systematic part. The random errors are caused by random device mismatches. Systematic errors can be considered as errors in the design. In CMOS op amp's, a major source of systematic errors is channel length modulation. Especially when short channels are used, channel length modulation will strongly affect the accuracy of current mirrors when the drain voltages of the mirror transistors are not equal. In an op amp, the result is an offset voltage and often a decrease of the common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR).

In this paper, a completely symmetrical two-stage operational amplifier design is presented, resulting in a very low systematic offset voltage and improved CMRR and PSRR. The paper is organized as follows. In section II the input/gain stage of the amplifier is presented. Next, in section III, a floating current source is presented which is required in the input stage. The output stage and gain boost amplifiers are discussed in sections IV and V, respectively.

II. The Input/Gain Stage

Fig. 1 shows the input/gain stage of the amplifier. Complementary differential pairs M_7, M_{10} and M_8, M_9 are connected in parallel to obtain a rail-to-rail common mode input range. For high common-mode voltages only the n-type differential pair operates and for low common-mode voltages only the p-type differential pair operates. The tail currents I_{b1} and I_{b2} of these differential pairs are dependent on the common-mode input voltage [1] in such a way that the transconductance of the complete input stage remains constant for all common-mode levels. An input stage of this type requires a low input offset voltage because differences in the offset voltages of the two differential pairs have an immediate impact on the CMRR of the amplifier [1,2,3,4].

Current mirrors M_3, M_4, M_5, M_6 and M_{11}, M_{12}, M_{15}, M_{16} are used to eliminate the common-mode voltage dependent bias currents I_{b1} and I_{b2} and replace them by a constant bias current I_{fl}. This current has to be generated by a floating current source to obtain an optimal matching between the currents flowing through the upper and lower current mirrors.

Gain boost amplifiers (GBp and GBn) are often used to increase the open-loop gain of the amplifier without increasing the number of amplifier stages [5]. Normally, the non-inverting inputs of the gain-boost amplifiers are connected to a constant bias voltage. Connecting the amplifiers in the way shown in fig. 1

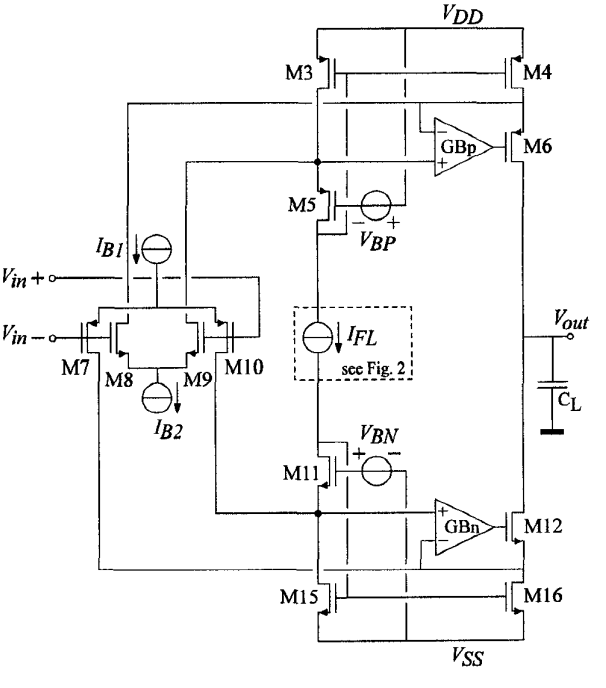

fig. 1 Input/gain stage.

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results in the same increase of the open-loop gain. Furthermore, a significant reduction of the systematic offset voltage is obtained, due to the improved matching between the drain voltages of transistor pairs M_3, M_4 and M_{15}, M_{16}.

III. Floating Current Source

The floating current source I_{FL} consists basically of two n-type and two p-type MOSFETs, which form a floating current mirror as indicated in fig. 2*(a)*. The input current I_S of this current mirror flows through M_4 and M_6. The level shift voltages V_{B1} and V_{B2} are inserted to reduce the voltage drop acros M_4 and M_6 and, thus, enable the circuit to operate at lower supply voltages. The voltages V_{B1} and V_{B2} are approximately equal to the threshold voltage of an n-type and p-type transistor, respectively. A differential amplifier senses the voltage level at the sources of M_{11} and M_{12} and adjusts the lower current source I_S in order to keep this voltage at a fixed level. The complete circuit implementation of the floating current source is shown in fig. 2*(b)*.

IV. Output Stage

A well-known class AB output stage [1], [6], [7] was used. Fig. 3 shows the output stage connected to of the input/gain stage. The output transistors M_{17} and M_{18} are class AB controlled by adding transistors M_{19} and M_{20} and bias voltages V_{CN} and V_{CP}.

Due to the class AB control, only a small quiescent current flows through the output transistors. For large signal currents, one of the output transistors is kept at a minimum current level, while the other output transistor provides the signal current. Also, in this situation only one of the gain boost amplifiers will contribute to the signal gain. For example, for a negative output voltage, the current through M_{18} will be large while M_{17} conducts a constant minimum current (M_{20} is turned off, all current coming from M_6 flows through M_{19}). The amplifier gain is now proportional to the impedance at the gate of M_{18}, which is mainly defined by the cascode stage consisting of M_{12} and gain boost amplifier GBn. Similarly, for positive output voltages the gain will be defined by M_6 and GBp.

Due to the difference between the device parameters of n-type and p-type MOSFETs, the gains of the two cascode stages, GBn,M_{12} and GBp,M_6, are generally not the same. The result is an increased distortion due to the asymmetrical gain. In the next section it will be shown that the gain boost amplifiers can be dimensioned in such a way that the overall amplifier gain becomes symmetrical.

V. The Gain Boost Amplifiers

For the output stage of fig. 3, the output resistance of the cascode stage consisting of M12, M16 and GBn can be approximated by:

$$Ro,n \approx A_{GBn} \cdot g_{m12} \cdot r_{o12} \cdot r_{o16}, \qquad (1)$$

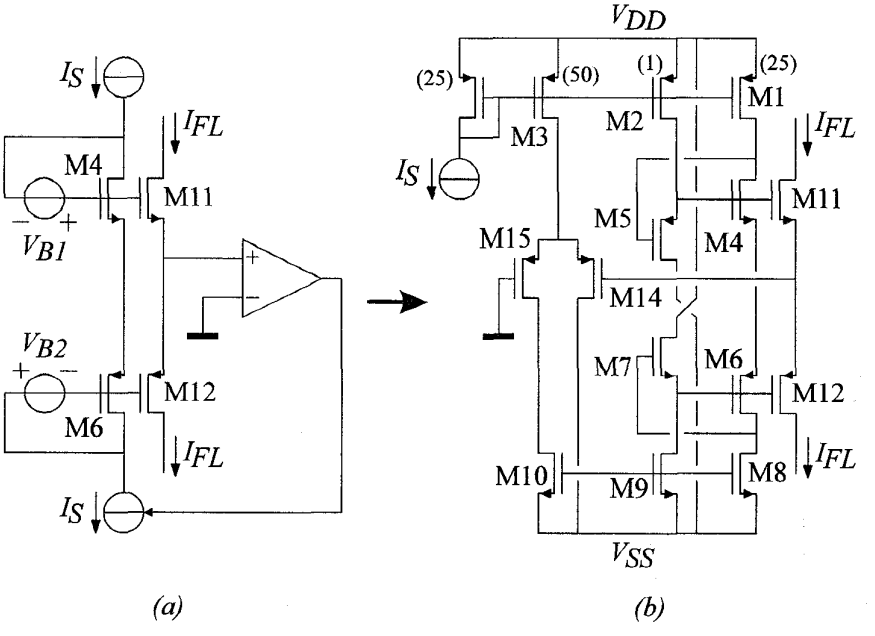

fig. 2 Floating current source: principle (a) and implementation (b).

where A_{GBn} is the dc gain of gain boost amplifier GBn. For the other cascode stage the output resistance can be expressed as:

$$Ro,p \approx A_{GBp} \cdot g_{m6} \cdot r_{o6} \cdot r_{o4}, \qquad (2)$$

where A_{GBp} is the dc gain of GBp. Due to the differences between n-type and p-type transistors $R_{o,n}$ and $R_{o,p}$ are not equal to each other, resulting in the asymmetrical amplifier gain.

Fig. 4 shows the implementation of the gain boost amplifiers as proposed in [5]. The gain of the gain boost amplifiers is determined by:

$$A_{GB} \approx g_{m101} \cdot [\,(g_{m105} \cdot r_{o105} \cdot r_{o103}) \,//\, (g_{m107} \cdot r_{o107} \cdot r_{o109})\,] \qquad (3)$$

When the drain source resistances of the saturated n-type MOSFETs M_{103} and M_{105} of GBn are chosen much larger than the drain source resistances of the p-type MOSFETs M_{107} and M_{109}, the product of the p-MOS parameters $g_{m107}r_{o107}$ and r_{o109} will determine the gain of the gain boost amplifier in the n-type cascode stage. The output resistance of the cascode stage (1) can then be approximated by :

$$Ro,n \approx g_{m101} \cdot g_{m107} \cdot r_{o107} \cdot r_{o109} \cdot g_{m12} \cdot r_{o12} \cdot r_{o16} \qquad (4)$$

Similarly, the output resistance of the p-type cascode stage (2) can be approximated by :

$$Ro,p \approx g_{m201} \cdot g_{m207} \cdot r_{o207} \cdot r_{o209} \cdot g_{m6} \cdot r_{o6} \cdot r_{o4} \qquad (5)$$

The transistor dimensions can now be chosen such that we obtain a symmetrical amplifier gain.

VI. Simulation and Measurement Results

Simulations have been performed using PSPICE with the level 3 MOS transistor model. The nominal supply voltage of the Op Amp was 3 Volts. The simulated minimum supply voltage was 2.2 Volts.

The simulations clearly show the expected improvement of the systematic offset voltage as a result of the floating current source I_{FL} and the special connection of the input terminals of the gain boost amplifiers. In fact, in the simulations the systematic offset vanishes completely.

The complete operational amplifier will be realized in our semi-custom CMOS process. Measurement results are expected at the time of the the conference.

VII. Conclusion

A low-voltage CMOS op amp with rail-to-rail input and output ranges has been presented. The amplifier contains a floating bias current source and specially connected gain boost amplifiers in order to minimize the systematic offset voltage. Furthermore, the gain boost amplifiers have been dimensioned in such a way that the overall amplifier gain is symmetrical for positive and negative output voltages.

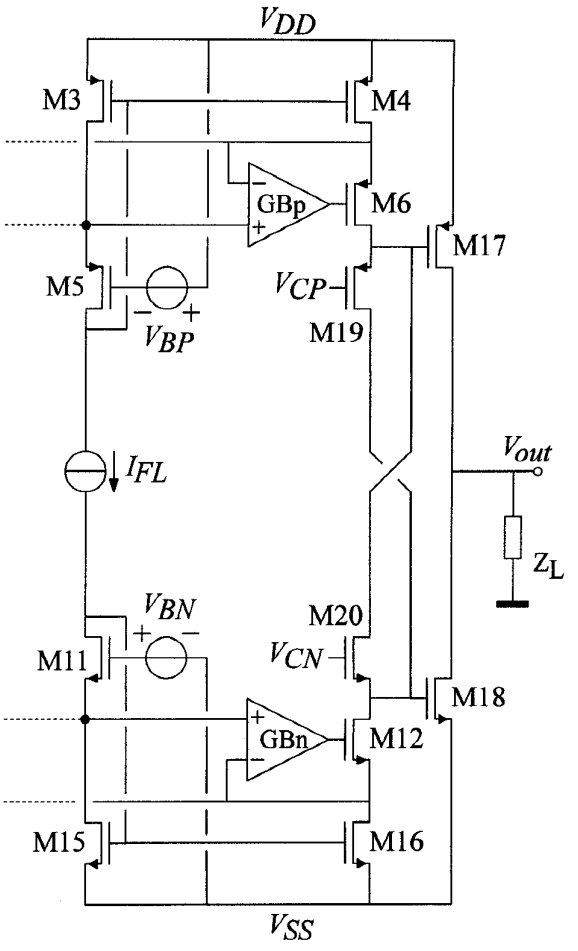

fig. 3 Class AB output stage.

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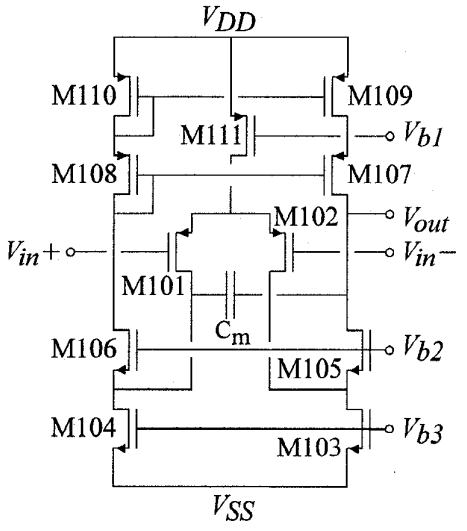
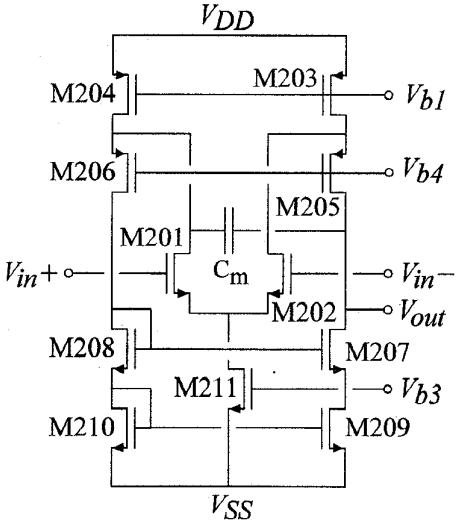
References

[1] J. H. Botma, R. J. Wiegerink, S. L. J. Gierkink, R. F. Wassenaar, "Rail-to-rail constant-gm input stage and class AB output stage for low-voltage CMOS Op Amps," *Analog Integrated Circuits and signal Processing*, 6, pp 121-133, 1994.

[2] M. D. Pardoen and M. G. Degrauwe, "A rail-to-rail input/output CMOS power amplifier," *IEEE J. Solid-State Circuits*, vol. 25, no. 2 pp. 501-504, Apr. 1990.



(a) GBn



(b) GBp

fig. 4 Implementation of the gain boost amplifiers GBn (a) and GBp (b).

[3] M. Steyaert and W. Sansen, "A high-dynamic-range CMOS Op Amp with low-distortion output structure," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 6, pp 1204-1207, Dec. 1987.

[4] F. op 't Eynde, P. Wambacq and W. Sansen, "On the relationship between the CMRR or PSRR and the second harmonic distortion of differential input amplifiers," *IEEE J. Solid-State Circuits*, vol. 24, no.6, pp 1740-1744, Dec. 1989.

[5] K. Bult and G. J. G. M. Geelen, "The CMOS gain boosting technique," *Analog Integrated Circuits and Signal Processing*, 1, pp.119-135, 1991.

[6] D. M. Monticelli, "A quad CMOS single-supply Op Amp with rail-to-rail output swing," *IEEE J. Solid-State Circuits*, vol. SC-21, no. 6, pp. 1026-1034, Dec. 1986.

[7] Wen-Chung S. Wu, Ward J. Helms, Jay A. Kuhn and Bruce E. Byrkett,"Digital-Compatible High-Performance Operational Amplifier with Rail-to- Rail Input and Output Ranges," *IEEE J. Solid-State Circuits*, vol. SC-29, no. 1, pp. 63-66, Jan. 1994.